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10/710,398	07/08/2004	Yung-Chun Lei	MTKP0068USA	4397

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EXAMINER	
YAARY, MICHAEL D	
ART UNIT	PAPER NUMBER
2193	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/710,398	LEI ET AL.	
	Examiner	Art Unit	
	MICHAEL YAARY	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-13,15-27 and 29-33* is/are rejected.

7)☒ Claim(s) *5,14 and 28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *07/08/2004 and 06/29/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-33 are pending in the application.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being unclear and indefinite. The claim, in line 19, recites the limitation "an arithmetic unit for processing the digital data." It is unclear as to which digital data is being processed. Is it the long-bit length digital data having fixed-point representation or the long bit-length digital data having jumping floating-point representation? Thus, "the digital data" in the limitation is lacking any antecedent basis.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-3, 10-12, 22-26, and 29-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Narita et al. (hereafter Narita)(US Pat. 5,293,558) in view of Nelson et al. (hereafter Nelson)(US Pat. 4,805,128).

6. **As to claim 1,** Narita discloses a digital signal processor for processing at least a digital data, the digital data having a plurality of representations (abstract), the representations including at least a floating-point representation (column 5, lines 10-12), the DSP comprising:

A multiplication circuit for multiplying at least two short bit-length data together to generate a long bit-length digital data (column 4, lines 29-39); and an arithmetic unit for processing the digital data (column 2, lines 49-64).

7. Narita does not disclose the representations including fixed point-representation; an extracting/shifting device electrically connected to the multiplication circuit for transforming a long-bit length digital data having the jumping-floating point representation into a long-bit length digital data having the fixed-floating point representation; and a plurality of representation converters, each of the representation converters transforming a specific digital data between the fixed-point representation and jumping-floating point representation through using a jumping-floating point arithmetic.

However, Nelson discloses the representations including fixed point-representation (abstract); an extracting/shifting device electrically connected to the

multiplication circuit for transforming a long-bit length digital data having the jumping-floating point representation into a long-bit length digital data having the fixed-floating point representation (column 1, line 49-column 2, line 16); and a plurality of representation converters, each of the representation converters transforming a specific digital data between the fixed-point representation and jumping-floating point representation through using a jumping-floating point arithmetic (column 1, lines 22-48).

8. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to modify, the teachings of Narita, by converting representations from fixed to floating-point and vice versa, as taught by Nelson, for the benefit of sharing components for conversions in both directions and further performing small and large scale calculations at high speeds.

9. **As to claim 2,** the combination of Narita and Nelson disclose a storage instrument electrically connected to the arithmetic unit for storing the digital data (Narita, column 4, lines 29-39).

10. **As to claim 3,** the combination of Narita and Nelson disclose the jumping-floating point arithmetic is used for transforming a long bit-length digital data having the fixed-point representation into a short bit-length digital data having the jumping floating-point representation, or is used for transforming the short-bit length digital data having the jumping floating-point representation into the long bit-length digital data having the

fixed-point representation (Narita, column 4, lines 29-39 and column 5, line 10-column 6, line 25 disclose arithmetic calculations done on short and long bit-length data; and Nelson, column 1, lines 22-35 disclose converting between the two formats of fixed and floating point. Thus, when taken in combination Narita and Nelson disclose converting short or long digital data between the two different formats.).

11. **As to claim 10,** the combination of Narita and Nelson disclose an enabling control signal used for controlling if the extracting/shifting device and the representation converters are enabled (Nelson, column 12, lines 23-24).

12. **As to claim 11,** the combination of Narita and Nelson disclose the arithmetic unit is used for processing the digital data having the fixed-point representation (Narita, column 2, lines 49-64; column 4, lines 29-39; and column 5, line 10-column 6, line 25 disclose arithmetic calculations done on short and long bit-length data; and Nelson, column 1, lines 22-35 disclose converting between the two formats of fixed and floating point. Thus, when taken in combination Narita and Nelson disclose converting short or long digital data between the two different formats and performing arithmetic calculations.).

13. **As to claim 12,** the combination of Narita and Nelson disclose a data receiving end for receiving the digital data (Narita, column 3, lines 13-19); and a data writing-in

end for storing a short bit-length digital data having the jumping floating-point representation into memory device (Nelson, column 5, line 63-column 6, line 5).

14. **As to claim 22,** the claim is rejected for similar reasons as applied to claims 1, 3, and 12 above.

15. **As to claim 23,** the combination of Narita and Nelson disclose each digital data comprises a sign bit (Nelson, abstract).

16. **As to claim 24,** the combination of Narita and Nelson disclose each short-bit length digital data having the jumping floating-point representation comprises a tail mark (Nelson, column 1, line 49-column 2, line 11).

17. **As to claim 25,** the combination of Narita and Nelson disclose the first representation converter transforms the short bit-length digital data having the jumping floating-point representation into the long bit-length digital data having the fixed-point representation according to the tail mark and the sign bit of the short bit-length digital data having the floating-point representation (Nelson, column 1, line 49-column 2, line 16).

18. **As to claim 26,** the combination of Narita and Nelson the extracting/shifting device transforms the long-bit length digital data having the jumping floating-point

representation into the long bit-length digital data having the fixed-point representation according to the tail mark of the two short bit-length digital data having the jumping floating-point representation (Nelson, column 1, line 49-column 2, line 16).

19. **As to claim 29,** the combination of Narita and Nelson disclose the extracting/shifting device, the first representation converter, and the second representation converter, are electrically connected to at least an enabling control signal, and the enabling control signal is used for controlling if the extracting/shifting device, the first representation converter, and the second representation converter are enabled (Nelson, column 12, lines 23-24).

20. **As to claim 30,** the combination of Narita and Nelson disclose the first representation converter transforms the short bit-length digital data having the jumping floating-point representation into the long bit-length digital data having the fixed point-representation when the enabling control signal enables the first representation converter, and the first representation converter transforms the short bit-length digital data having the fixed-point representation into the long bit-length digital data having the fixed-point representation when the enabling control signal disables the first representation converter (Nelson, column 34, lines 52-65).

21. **As to claim 31,** the combination of Narita and Nelson disclose the second representation converter transforms the long bit-length digital data having the fixed-point

representation into the short bit-length digital data having the jumping floating-point representation when the enabling control signal enables the second representation converter transforms the long bit-length digital data having the fixed-point representation into the short bit-length digital data having the fixed-point representation when the second enabling control signal disables the second representation converter (Nelson, column 34, lines 52-65).

22. **As to claim 32,** the combination Narita and Nelson disclose the multiplexing arithmetic module is used for selecting and computing at least a long-bit length digital data having the fixed point representation (Nelson, column 24, lines 24-35 and column 34, lines 52-65).

23. **As to claim 33,** the combination of Narita and Nelson disclose representations further comprise an integer representation (Nelson, column 38, lines 31-35).

24. Claims 4, 6-9, 13, 15-21 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Narita and Nelson as applied to claim 3 above, and further in view of Urano et al. (hereafter Urano)(US Pat. 5,317,526).

25. **As to claim 4,** the combination of Narita and Nelson do not disclose performing a magnifying shift to shift N bits of the long bit-length digital data having the jumping

floating-point representation according to an absolute value of the long-bit digital data wherein N is an integer not less than zero, eliminate a predetermined number of bits, and set up a tail mark to generate the short bit-length digital data having the jumping floating-point representation.

However, Urano discloses performing a magnifying shift to shift N bits of the long bit-length digital data having the jumping floating-point representation according to an absolute value of the long-bit digital data wherein N is an integer not less than zero, eliminate a predetermined number of bits, and set up a tail mark to generate the short bit-length digital data having the jumping floating-point representation (Abstract and column 2, line 59-column 3, line 46 disclose a method for converting a double precision floating-point number into single precision; thus reducing the long-bit digital data into short-bit digital data.).

26. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Narita and Nelson, by reducing the bit length of the digital data, as taught by Urano, for the benefit of increasing efficiency and processing speed.

27. **As to claim 6,** the combination of Narita, Nelson, and Urano disclose the jumping floating-point arithmetic includes a plurality of displacement modes and each one corresponds to a different value of N (Urano, column 2, line 59-column 3, line 2).

28. **As to claims 7 and 16,** the combination of Narita, Nelson, and Urano disclose each digital data comprise one sign bit, and a shifting mode and a value of N corresponding to the shifting mode are determined by comparing the sign bit with other bits of the long bit-length digital data (Urano, column 3, lines 27-46).

29. **As to claims 8 and 17,** the combination of Narita, Nelson, and Urano disclose the jumping floating-point arithmetic transforms the short bit-length digital data having the jumping floating-point arithmetic into the long bit-length digital data having the fixed-point arithmetic according to the tail mark and the sign bit. (It would have been obvious to one of ordinary skill in the art to utilize the floating-point to fixed and vice versa conversions as taught by Nelson, and the reduction arithmetic as taught by Urano; when taken in combination with the arithmetic processing teachings of Narita to transform short bit-length to long bit-length and vice versa.).

30. **As to claim 9,** the combination of Narita, Nelson, and Urano disclose when the two short bit-length digital data inputted into the multiplication circuit correspond to the jumping floating point representation, the extracting/shifting device transforms the long-bit length digital data having the jumping floating-point representation into the long bit-length digital data having the fixed-point representation according to tail marks of the two short bit-length digital data having the jumping-floating point representation (Nelson, column 1, line 49-column 2, line 16).

31. **As to claims 13 and 19,** the claims are rejected for similar reason as in claim 4 above.

32. **As to claim 15,** the claim is rejected for similar reasons as applied to claims 4 and 6 above.

33. **As to claim 18,** the combination of Narita, Nelson, and Urano disclose after step c, storing the short bit-length digital data having the jumping floating-point representation into a memory device (Narita, output register 113 of figure 4.)

34. **As to claims 20 and 21,** the claim is rejected for similar reason as claims 6 and 7 above.

35. **As to claim 27,** the combination of Narita and Nelson do not disclose performing a magnifying shifting to shift N bits of the long-bit length digital data having the fixed-point representation wherein N is an integer not less than zero, eliminates a predetermined number of bits, and sets up a tail mark to generate the short bit-length digital data having the jumping floating-point representation.

However, Urano discloses performing a magnifying shifting to shift N bits of the long-bit length digital data having the fixed-point representation wherein N is an integer not less than zero, eliminates a predetermined number of bits, and sets up a tail mark to

generate the short bit-length digital data having the jumping floating-point representation (Abstract and column 2, line 59-column 3, line 46 disclose a method for converting a double precision number into single precision; thus reducing the long-bit digital data into short-bit digital data; and when taken in combination with the teachings of Narita and Nelson can be applied to fixed-point representation.).

36. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Narita and Nelson, by reducing the bit length of the digital data, as taught by Urano, for the benefit of increasing efficiency and processing speed.

Allowable Subject Matter

37. Claims 5, 14, and 28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MICHAEL YAARY whose telephone number is (571)270-1249. The examiner can normally be reached on Monday-Friday, 8:00 a.m - 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lewis Bullock can be reached on (571) 272-3759. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/M. Y./
Examiner, Art Unit 2193

/Lewis A. Bullock, Jr./
Supervisory Patent Examiner, Art Unit 2193